**WHAT IS CLAIMED IS:**

1. In a semiconductor package comprising a semiconductor die having a plurality of interconnect pads positioned thereon and at least one group of interconnect pads, the at least one group of interconnect pads comprising:

a victim interconnect pad configured to carry a signal that is susceptible to noise created by surrounding signals; and

shield interconnect pads functioning as shields to the victim interconnect pad, at least four of the shield interconnect pads being positioned near the victim interconnect pad and closer to the victim interconnect pad than other noise sources from external to the semiconductor die wherein the at least four of the shield interconnect pads form a noise shield within a periphery of the victim interconnect pad.

2. The semiconductor package of claim 1 wherein each of the at least four of the shield interconnect pads is an interconnect for ground or power.

3. The semiconductor package of claim 1 wherein the victim interconnect pad conducts a signal that is sensitive to noise.

4. The semiconductor package of claim 1 wherein the four interconnect shield pads are respectively positioned in each of four quadrants surrounding the victim interconnect pad.

5. The semiconductor package of claim 4 wherein each of the four interconnect shield pads is positioned a predetermined distance from a center of the victim interconnect pad and substantially at each corner of a square centered on the victim interconnect pad.

6. The semiconductor package of claim 1 further comprising a bond wire connected to each of the victim interconnect pad and the shield interconnect pads.

7. The semiconductor package of claim 6 wherein each bond wire that is connected to each of the victim interconnect pad and the shield interconnect pads is routed to a support

structure while maintaining a shield structure around the bond wire connected to the victim interconnect pad.

8. The semiconductor package of claim 7 wherein the shield structure further comprises a physical arrangement of bond wires electrically connected to the shield interconnect pads to form a cage substantially around the bond wire electrically connected to the victim interconnect pad, the bond wires electrically connected to the shield interconnect pads being closer to the bond wire electrically connected to the victim interconnect pad than other noise sources radiating from bond wires of the semiconductor package.

9. The semiconductor package of claim 1 wherein the victim interconnect pad further comprises two victim interconnect pads positioned adjacent to each other and surrounded by the shield interconnect pads.

10. The semiconductor package of claim 9 wherein the two victim interconnect pads conduct a differential signal.

11. The semiconductor package of claim 1 wherein a first portion of the plurality of interconnect pads is positioned to a first side of the one group of interconnect pads along a peripheral edge of the semiconductor die and a second portion of the plurality of interconnect pads is positioned to a second side of the one group of interconnect pads along the same peripheral edge of the semiconductor die.

12. The semiconductor package of claim 1 further comprising:
eight interconnect shield pads that are respectively positioned surrounding the victim interconnect pad.

13. The semiconductor package of claim 12 wherein the eight interconnect shield pads are positioned substantially adjacent to each of four sides of the victim interconnect pad and offset from each of four corners of the victim interconnect pad.

14. A semiconductor package comprising:
a support structure;

a semiconductor die overlying the support structure;

a plurality of interconnects electrically connecting the support structure and the semiconductor die; and

at least one shielding group of interconnects that electrically shield a predetermined victim interconnect from noise sources, the at least one shielding group of interconnects comprising at least four interconnects surrounding a periphery region of the victim interconnect and being positioned closer to the victim interconnect than any of the plurality of interconnects.

15. The semiconductor package of claim 14 wherein the at least four interconnects are positioned such that any closest noise source to the victim interconnect is at least 1.5 times a closest bond pad pitch to the victim interconnect.

16. The semiconductor package of claim 14 wherein the at least four interconnects further comprise four interconnects respectively positioned in each of four quadrants encompassing a periphery of the victim interconnect.

17. The semiconductor package of claim 14 wherein the at least four interconnects further comprise eight interconnects substantially surrounding the periphery of the victim interconnect and are located closer to the victim interconnect than any aggressor interconnect of the semiconductor package.

18. The semiconductor package of claim 14 wherein each interconnect of the at least one shielding group of interconnects further comprise an interconnect pad located on the semiconductor die and a respective connected bonding wire that forms a portion of a bonding wire cage that exists from the semiconductor die to a predetermined site on the support structure.

19. The semiconductor package of claim 14 wherein the victim interconnect further comprises two victim interconnects positioned adjacent to each other and the two victim interconnects are surrounded by each interconnect of the shielding group of interconnects.

20. The semiconductor package of claim 19 wherein the two victim interconnects conduct a differential signal.

21. A method of noise isolation in a semiconductor comprising:

providing a support structure;

providing a semiconductor die overlying the support structure;

providing a plurality of interconnects electrically connecting the support structure and the semiconductor die;

providing at least one shielding group of interconnects that electrically shield a predetermined victim interconnect from noise sources; and

positioning at least three interconnects around a periphery region of the victim interconnect and closer to the victim interconnect than any of the plurality of interconnects.